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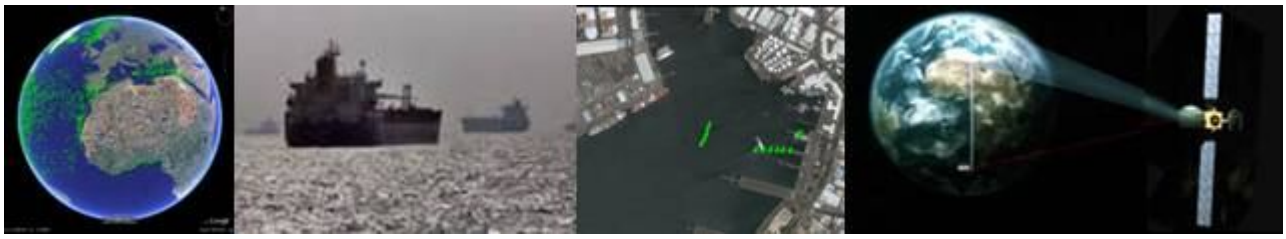
Flight Operations



Technical Note TN-09:

Critical Review of ESA proposed Design and Software

Preparatory Action for Assessment of the Capacity of Spaceborne Automatic Identification System Receivers to Support EU Maritime Policy

DG MARE Service Contract MARE/2008/06 – SI2.517298

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1	09.11.2009	COM DEV	Including comments from LXS
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Applicable and Reference Documents

RD 1	Preparatory Action for Assessment of the Capacity of Spaceborne Automatic Identification System Receivers to Support EU Maritime Policy – Pasta Mare Technical Proposal Call for Tenders No MARE/2008/06

TABLE OF CONTENT

1. INTRODUCTION

This document presents the Pasta Mare consortium's consolidated initial review of the supplied ESA algorithm and also presents the hardware platform via which the algorithm will be practically evaluated.

2. ESA ALGORITHM REVIEW

2.1 SCOPE

The aim of this section is to present the results obtained from the different tests carried out in order to assess the performance of the receiver proposed by ESA and its suitability for the PASTA MARE project.
The ESA Advanced Receiver has been designed to detect AIS signals from LEO satellites. The provided code, programmed in MATLAB, consists of an AIS modem, AIS messages are generated with random bits and GMSK modulated. After including the channel effect (AWGN noise, Doppler shift, interferences,…) the demodulator starts the detection.
The performed tests and the achieved results are described in the following sections.

2.2 BER PERFORMANCE

The modulator is used to generate signals within the E_b/N_0 range: [0, 11] dB. No delay is considered. The Doppler shift chosen is 10 Hz to keep a small value but also not an ideal one like 0 Hz. In the code, a collider with a -30 dB power w.r.t. the main signal is included too. This can be considered a non-collision scenario since the collider is negligible with respect to the main signal.

Figure 1 shows the receiver performance in this case (blue line). The red line represents the theoretical BER performance achieved by a GMSK coherent demodulator with BT = 0.4. As can be seen the receiver proposed by ESA has only 1 dB loss compared to the theoretical results.

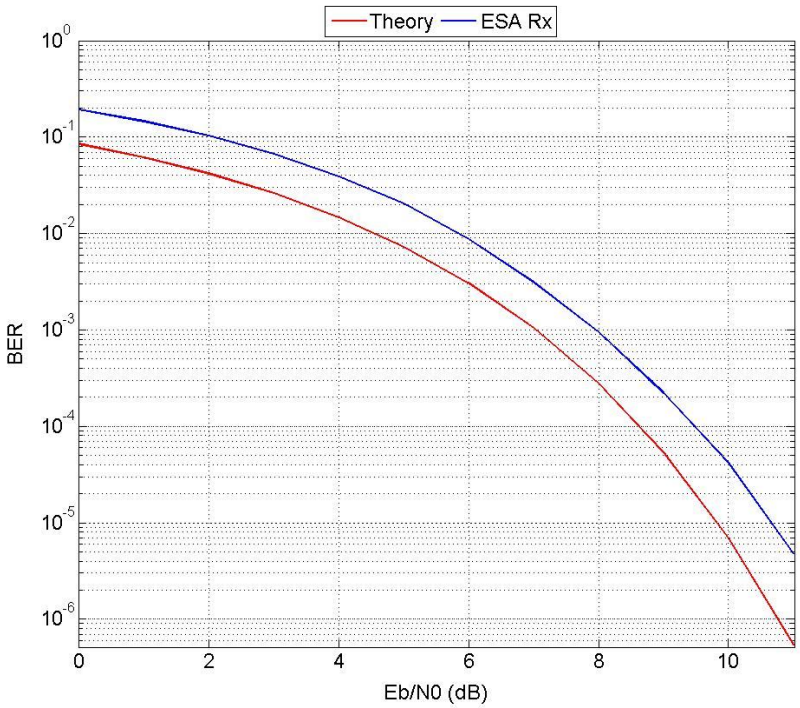

Figure 1: BER performance of ESA receiver considering as input signal a main frame and a collider with -30 dB power w.r.t the main signal

2.3 PERFORMANCE IN THE DOPPLER FREQUENCY RANGE

For this test, signals with different Doppler shifts are generated in order to handle the expected Doppler range for satellite reception: ±4 kHz approximately. The E_b/N_0 of the frames is 10 dB and no delay is considered. There is no collision.

The result is depicted in Figure 2. As can be seen, the receiver has very low BER around the range [−1.5, 1.5] kHz but very high outside of it. This is the expected range according to [1] since the code provided corresponds only to a *zonal demodulator*, handling Doppler shifts up to 15% of the data rate (±0.15·9600 = ±1440 Hz).

For the speed of the aircraft, the maximum Doppler shift is a few hundreds Hertz, which would be in the interval covered by a zonal demodulator. However, some AIS real signals present a frequency shift of up to ±2 kHz due to the tolerance of the components used in the AIS transmitter onboard the ship. Therefore, the three zonal demodulators, as proposed in [1], are required. The integration of the three parallel demodulators is not included in the code and needs to be implemented.

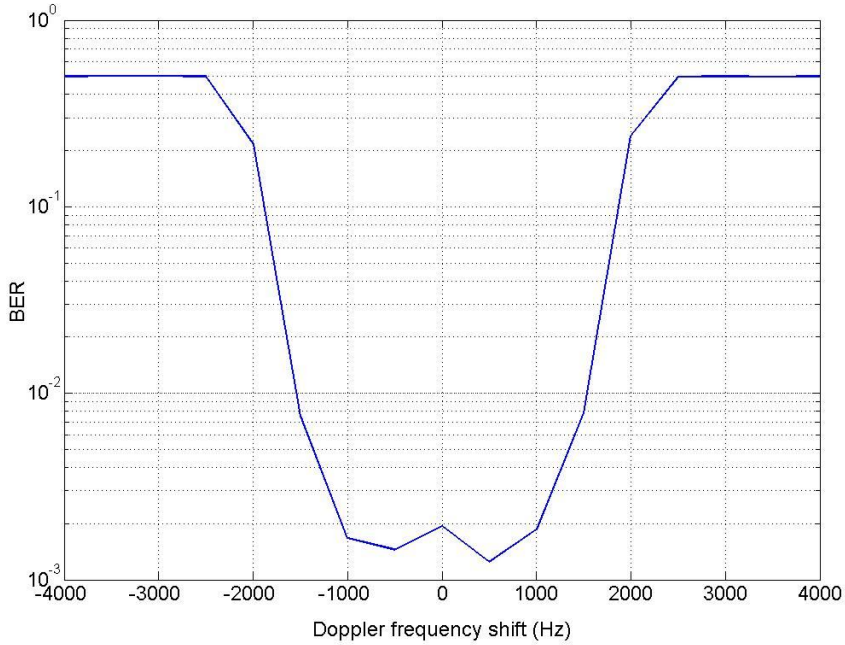

Figure 2: Performance of the Advanced Receiver proposed by ESA in the spaceborne AIS frequency range.

2.4 COLLISION SCENARIO

The purpose of this test is to assess the BER performance of the ESA receiver in the collision scenario. Two examples are considered: a) main signal and collider with −4 dB w.r.t. the main frame and b) main signal and collider with −10 dB w.r.t. the main frame. The main signal has 2 Hz Doppler and no delay. The collider has 500 Hz Doppler and no delay. The results obtained are presented in Figure 3. The red line represents again the theoretical BER performance achieved by a GMSK coherent demodulator. The blue line corresponds to the ESA receiver BER performance for the -10dB collider and the black line corresponds to the −4dB collider. This shows that, for the −4dB collider case, the probability to recover at least one of the messages is very low. In the case of 10 dB Signal-to-Collider the loss w.r.t the theoretical results is 8 dB.

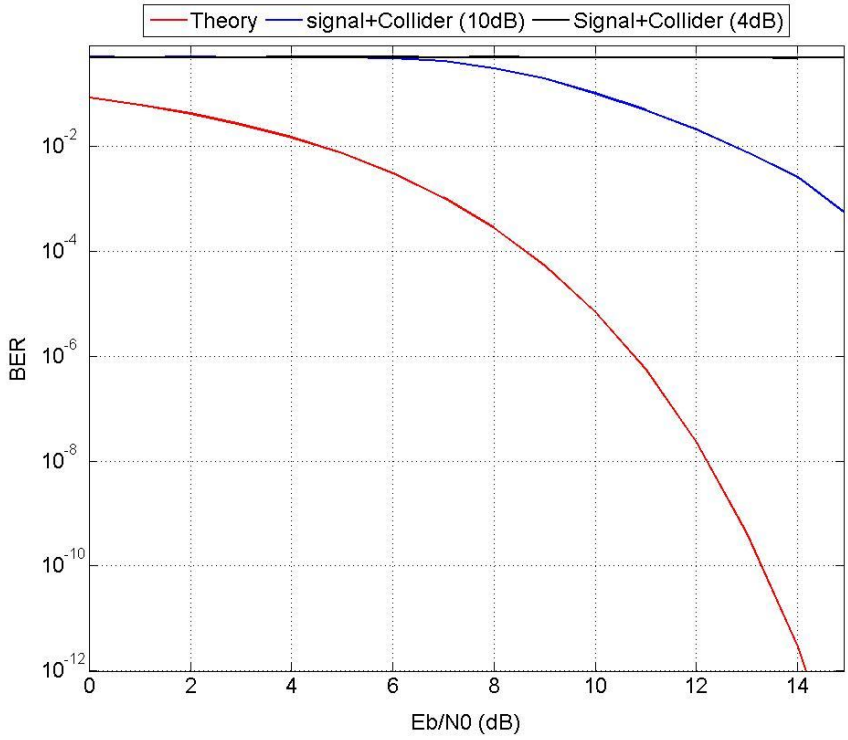

Figure 3: ESA Receiver Performance in case of Collision (Colliders have −4dB power and −10dB power w.r.t main signal)

2.5 SYNTHESIZED AND REAL SIGNALS

The ESA receiver has been modified to be tested with computer generated signals and with real signals. The ESA Advanced Receiver code is able to demodulate them. However, it requires an additional implementation to identify the beginning of the Time Slot and to extract the message information (bit de-stuffing and byte inversion).

Therefore, the receiver performance for real signals can not be compared with the curve shown in above.

2.6 INTERFERENCE CANCELLATION (RE-MODULATION)

The ESA algorithm is based upon the well known technique of Sequential Interference Cancellation (SIC). It scans the decoded bits from the first-stage Detector until a CRC match is obtained. The resulting “good” frame is then used as a reference in order to estimate timing, frequency, amplitude and phase using well known data-aided estimation algorithms. The reference is re-modulated then subtracted from the input signal vector. A second detection attempt using the cancelled signal is then attempted.

In the MATLAB code, no first-stage detection is actually used; instead the originally transmitted bit-sequence is used directly as the reference i.e. as a-priori knowledge. The justification is presumably on the basis of saving simulation time. However, given the rather poor performance presented in Figure 3-3 for the case of a 4dB C/I ratio, it is unlikely the first-stage detection would succeed such that a good CRC and hence reference waveform could be obtained.

2.7 SUITABILITY FOR REAL-TIME EXECUTION

The ESA algorithm makes use of well tried-and-tested algorithms such as the 2 state non-coherent Viterbi Decoder to detect a GMSK signal based on the Laurent waveform decomposition principle and familiar estimators based on autocorrelation estimation. As such, the algorithms themselves are suitable for implementation in an FPGA possibly in conjunction with a CPU or state machine logic to control the state transitions necessary to organise the execution of the algorithms and post-process the frames for AIS (not currently part of the algorithm).

The use of three zonal demodulators is convenient for firmware execution as either three parallel sets of algorithms – or more likely a single zonal demodulator used three times in the course of processing a frame. The memory needs of the algorithm may be significant as buffers to hold up to three AIS frames at a time may be required for detection and interference cancellation. Depending upon the implementation, the memory may need to be replicated three times for the three zonal demodulators.

The MATLAB code in its present form is not suitable for execution even in non-real time on a mission (e.g. the flight trial) as it is lacks a means to synchronise to captured data. In the case of interference cancellation (re-modulation), the first stage detection would have to be enabled as clearly there would be no a-priori knowledge. The algorithm does not appear to make use of the 24 bit preamble or HDLC flags for initial channel estimation.

2.8 CONCLUSIONS ON THE ESA ALGORITHM

The ESA algorithm uses well established techniques which are amenable to firmware or software implementation and possesses the expected performance for a MLSE-based GMSK signal detector with non-data-aided timing and frequency estimation. The performance in the presence of interference, based on the MATLAB simulation results may be insufficient to gain the full benefit of interference cancellation but this is FFS.

The MATLAB model in its present form is not suitable for in-flight processing and would need more work to enable it to be compiled to the flight platform. However, it could be usefully employed for post-flight data processing.

3. HARDWARE PLATFORM FOR AIS DATA CAPTURE

3.1 INTRODUCTION

The following section presents the hardware platform which will be used to capture the AIS data from the air. It is not intended to process the data real time, the hardware platform will enable the AIS data from the complete flight to be recorded and then later this data can be processed through the ESA algorithm to characterise its performance. It should also be noted that the hardware will include a battery pack to allow the platform to operate independent of any aircraft supplies.

3.2 HARDWARE DESCRIPTION

The block diagram of the hardware is shown in Figure 4-1. It consists of the following key elements

- RF Front End
  - Low Noise Amplifier/Splitter
  - Dual receiver (for the two AIS Channels at 161.975MHz and 162.025MHz)
- Radio Interface Board
- eInstrument Embedded PC
- Battery Pack

These elements are described in the following sections.

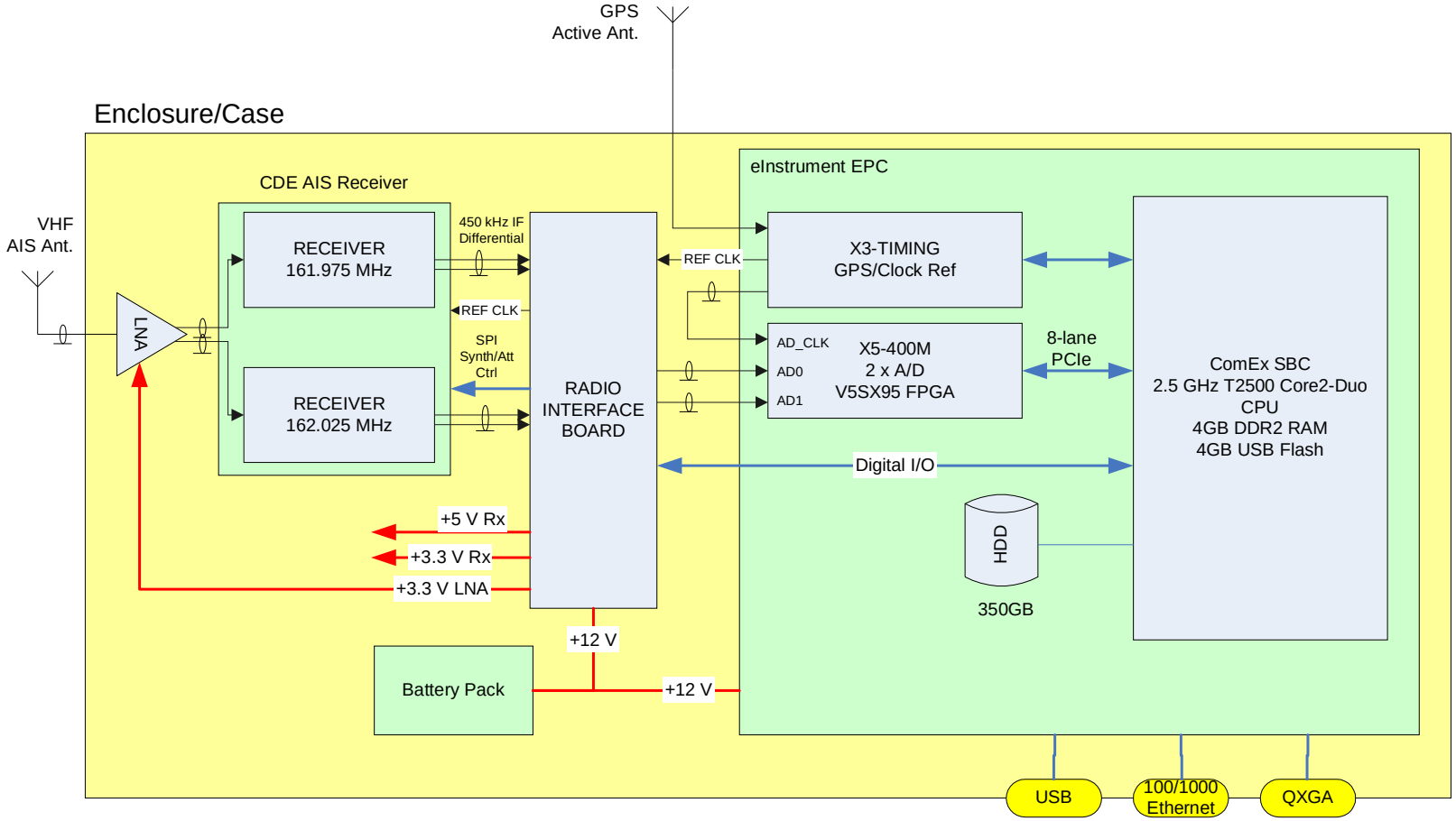

Figure 3: System Block Diagram

3.2.1 RF FRONT END

The RF Front end is directly derived from the systems developed by COM DEV for AIS reception from space. The LNA includes a specially designed front end SAW filter to limit the interference introduced to the front end of the LNA. It is a dual down-conversion receiver with the output to the interface board being at 450 kHz. The overall key front-end performance parameters are summarised in Table 5.

Parameter	Performance	Comments
Noise Figure (dB)	<3.5	Includes input SAW filter
Simultaneous Dynamic Range (dB)	> 55	
Eb/No (dB)	> 8	At –120dBm input level, 9600 bps
AIS Channel-Channel Isolation (dB)	> 50	

Table 5: Key RF Front-End Performance Parameters

The RF Front-end is shown in Figure below.

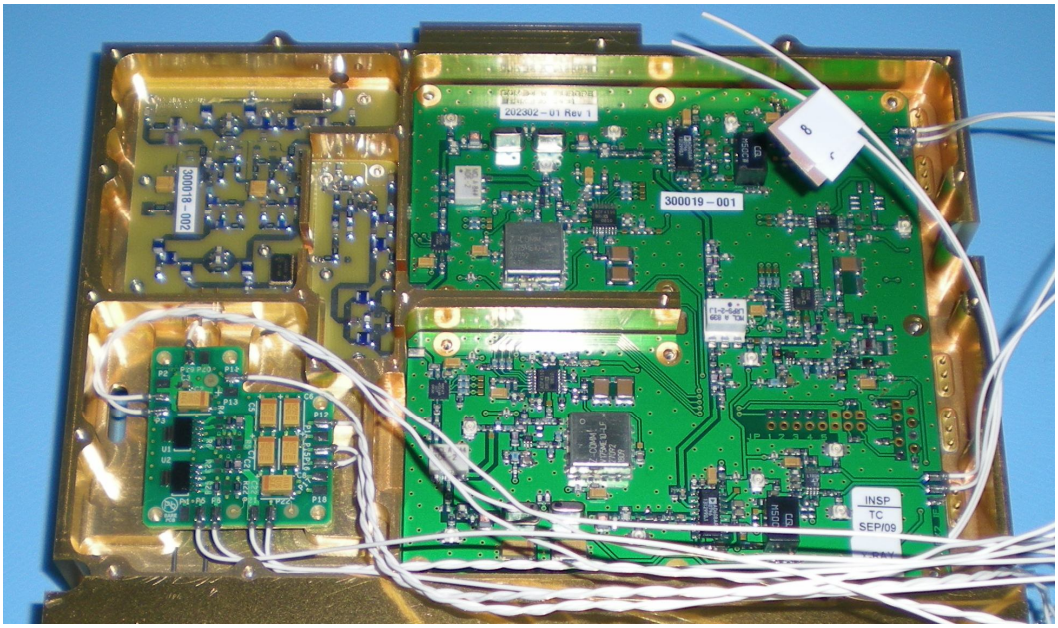

Figure 6: RF Front-End

3.2.2 RADIO INTERFACE BOARD

The radio interface board is the direct interface between the RF Front-end and the embedded processor. It performs the following key functions:

- Differential to single-ended conversion of IF output

- PLL Reference clock – derived from X5-400M system high stability reference – distributed to receiver
- SPI serial interfaces for programming 3 frequency synthesizers and two attenuators
- Power conditioning: +12 V in, 3.3 V (LNA) 3.3 V and +5 V (for receiver)

3.2.3 EMBEDDED PC

The embedded PC is an eInstrument PC (see Figure) which has the following functionality:

- Duo-core 2.5 GHz processor
- 4GB RAM
- 350GB HDD
- 8 Lane PCI express
- Windows XP Professional
- General purpose TTL compatible I/O

Figure 7: eInstrument-PC

The PC is fitted with two interface cards, the X400M and X3-Timing and the functions of these are detailed below:

X400M

The X400M (see Figure 8-1) has the following key features:

- Two 400 MSPS, 14-bit ADS5474 A/D channels
- Two 500 MSPS, 16-bit DAC channels
- +/-1V, 50 ohm, SMA inputs and outputs
- Xilinx Virtex5, SX95T FPGA
- 512 MB DDR2 DRAM
- 4 MB QDR-II SRAM
- 8 Rocket IO private links, 2.5 Gbps each

- >1 GB/s, 8-lane PCI Express Host Interface
- PCI Express (VITA 42.3)

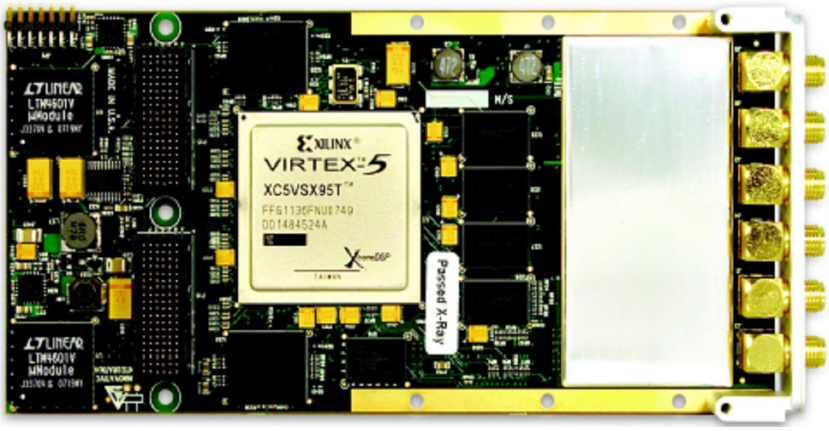

Figure 8-1: X400M Interface Card

X3-Timing

The X3-Timing (see Figure 8-2) has the following key features: -

- GPS Receiver
- Low noise high stability 10 MHz reference
- A/D sampling clock
- PCI Express (VITA 42.3)

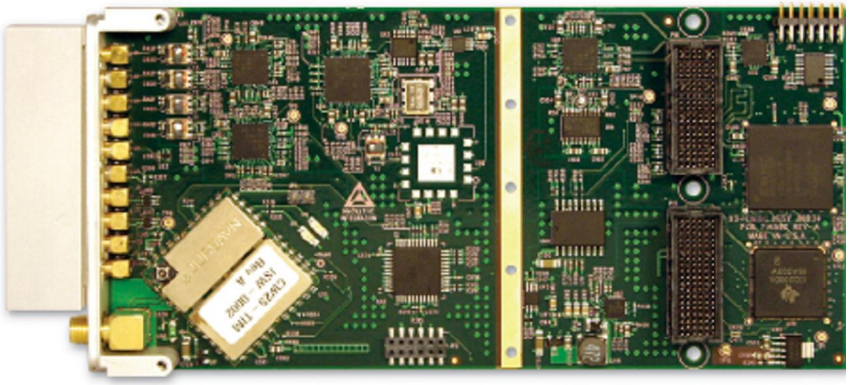

Figure 8-2: X3-Timing Interface Card

3.2.4 BATTERY PACK

The battery pack is integral with the hardware. This will enable the hardware to be operated on the plane without any connection to the power system of the plane itself.

3.3 SYSTEM DESCRIPTION

After reception from an external antenna the input signal is amplified by the low noise amplifier which is limited to bandwidth of approximately 2 MHz centred on 162 MHz by a specifically designed input SAW filter.

At the output of the LNA there is a 3dB splitter which feeds two receiver chains, one for each AIS channel (161.975MHz and 162.025MHz). The output of the each chain of the receiver is 450 kHz, which is fed via the Radio interface board to the input A/Ds of the X400M card.

Implemented in the Xilinx Virtex 5 FPGA is COM DEV's standard demodulation package, which has been utilised on a number of previous programmes. This package samples the 450 kHz IF at 1.80Msps using an Fs/4 demodulator and then subsequently decimates and filters to a ±12.5 kHz channel.

This results in an output sample rate at 28.125 ksps with a 12 bit I and 12 bit Q per channel. The 28 ksps output rate could be easily resampled to 200 ksps if required for compatibility reasons but would not provide any more signal resolution so it is not proposed to implement this.

This data is stored onto the embedded pc hard drive together with timestamp and GPS position data derived from the X3-timing card.

After the trial the data will be processed through the supplied ESA algorithm (with the updates suggested in section 2).

4. REFERENCES

[1] ESA Advanced Receiver Design for Satellite-based AIS Signal Detection