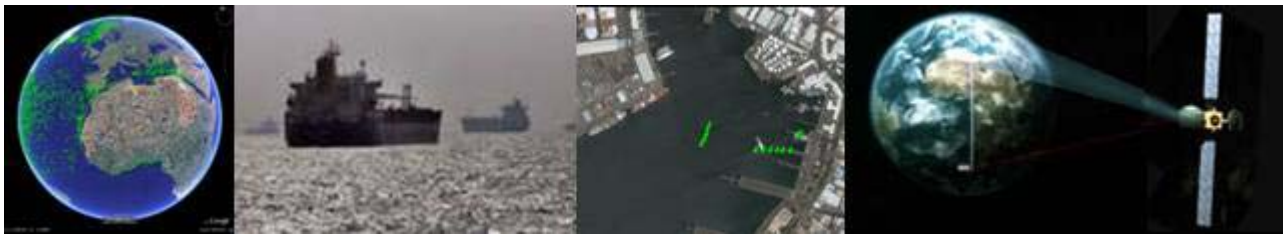
in cooperation with

Institute of
Space Systems

Flight
Operations



Technical Note TN-11-1:
Receiver Hardware ICD

Preparatory Action for Assessment of the Capacity of Spaceborne Automatic Identification System Receivers to Support EU Maritime Policy

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Title: **Receiver Hardware ICD**			

	Name & Function	*Signature*	*Date*
Prepared by:	Thomas Bleckert Systems Engineer		06.04.2010
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1			
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2. INTRODUCTION

The AIS Hardware Platform is part of the Luxspace program (see AD1 for details on the requirements).
The AIS Receiver is intended to process the VHF input signals at one coaxial connector for the standard AIS Frequencies (Channel AIS1 161.975 MHz and AIS2 162.025 MHz) and read out the signals on two IF Interfaces.
The Radio Interface board and LNA are a part of the AIS Receiver self and provided IF levels for the Digital Section, Control Interfaces, Power Supply and Reference Clock for the AIS Receiver.
The Digital Section is intended to process the Data from IF input and store the proceed data.
The Battery Pack is the main power supply for the Receiver, Digital Unit and other Devices. This power supply works as discrete power supply without any connections to the aircraft.

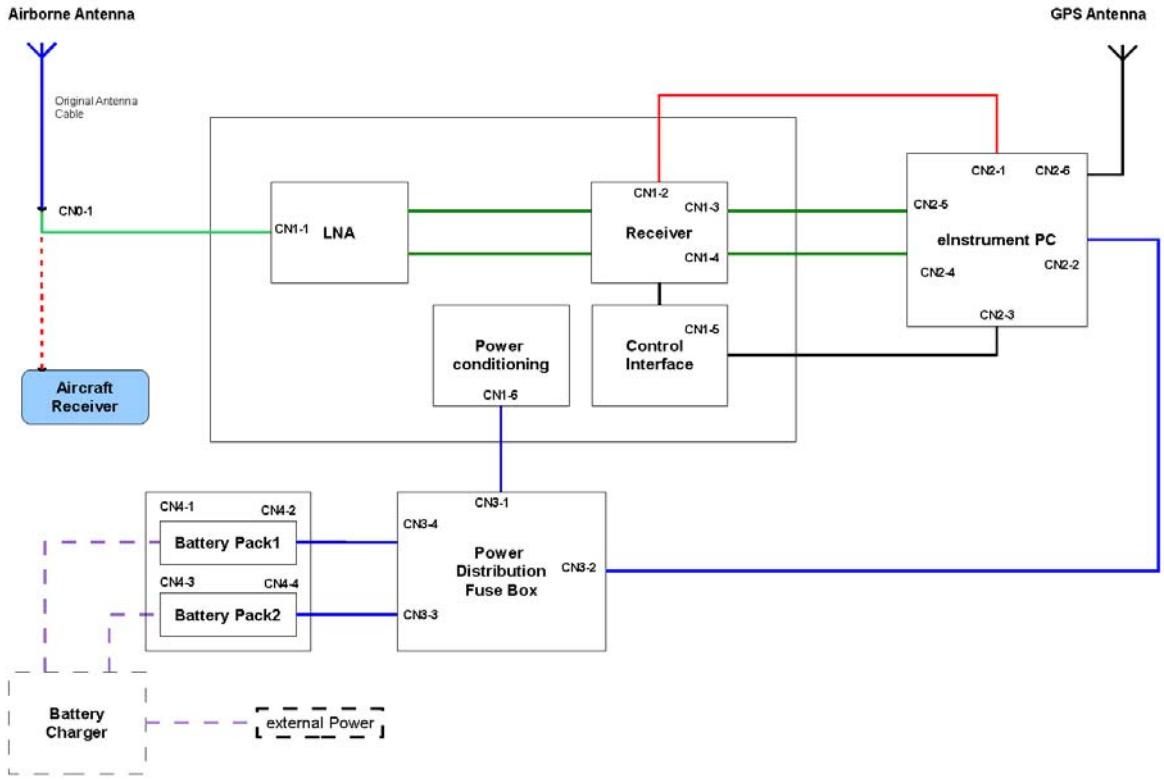

Figure 2-1 System Diagram

3. APPLICABLE AND REFERENCE DOCUMENTS

Document	Description
[AD-1]	6039 PASTA MARE Technical Note TN 09_Issue2.doc

Table 3-1: List of Applicable Documents

Document	Description
[AD-1]	Preparatory Action for Assessment of the Capacity of Space borne Automatic Identification System Receivers to Support EU Maritime Policy – Pasta Mare Technical Proposal Call for Tenders No MARE/2008/06

Table 3-2: List of Reference Documents

4. ABBREVIATIONS

The following abbreviations are used in this document.

Abbreviation	Full
Ah	Ampere Hour
AIS	Automatic Identification System
DC	Direct Current
GPS	Global Positioning System
IF	Intermediate Frequency
LNA	Low Noise Amplifier
PLL	Phase Locked Loop
RF	Radio Frequency
SPI	Serial Peripheral Interface Bus
TBC	To Be Confirmed
TBD	To Be Defined
VHF	Very High Frequency

Table 4-1: List of Abbreviations

5. INTERFACE DEFINITION

5.1 BATTERY PACK

HW-REQ-5.1.1.1 The Battery pack must have a protection against leakage (sealed construction).

HW-REQ-5.1.1.2 The Battery Pack shall be Shock and vibration resistant.

HW-REQ-5.1.1.3 The Battery Pack shall be supported to work in any position.

HW-REQ-5.1.1.4 The Battery Pack shall provide DC Power at 12 Volts and a Capacity from 80 Ah.

HW-REQ-5.1.1.5 The Battery Pack shall comprise a main Battery Pack and a redundant Battery Pack. Both shall be work in parallel without power cut.

HW-REQ-5.1.1.6 The Battery contacts shall have protection with electric insulating material against shorts.

HW-REQ-5.1.1.7 The Battery power cable shall be protected with a fuse close to the battery on the supply (+) side (Connector CN4-1, CN4-3)

HW-REQ-5.1.1.8 The Battery Pack shall use two different Battery connectors (ring tongues) for positive (supply) and negative (return) poles.

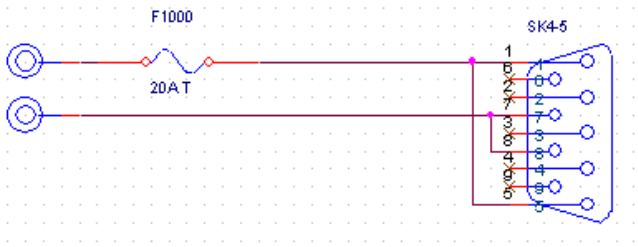

Figure 5-1 Battery Power Cable

Pin	Signal
1	+12V
2	
3	
4	
5	+12V
6	
7	RTN
8	RTN
9	

Table 5-1 Pin Out Connector CN4-1, CN4-3

HW-REQ-5.1.1.9 The Battery Pack shall use D-Sub 9-way sockets to distribute the power to the Power Distribution Box (Connector CN4-2, CN4-5)

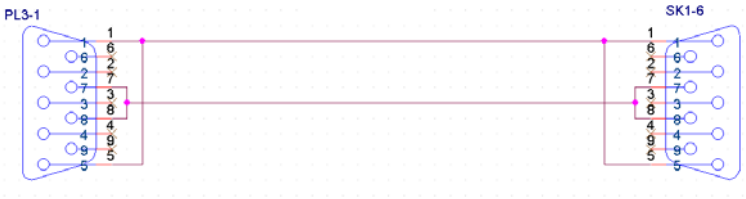

Figure 5-2 Distribution Cable

Pin	Signal
1	+12V
2	
3	
4	
5	+12V
6	
7	RTN
8	RTN
9	

Table 5-2 Pin Out Connector CN4-2, CN4-5

HW-REQ-5.1.1.10 The Power Distribution Box shall use D-Sub 9-way sockets to distribute the power to the Receiver (Connector CN3-1) and the eInstrument PC (Connector CN3-2)

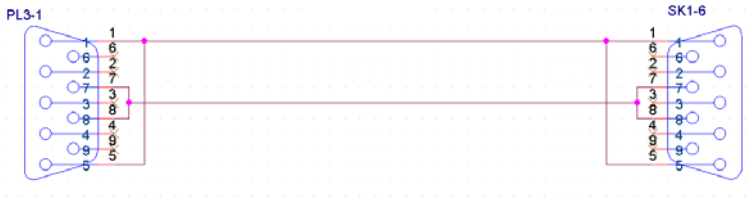

Figure 5-3 Power Cable to Receiver

Pin	Signal
1	+12V
2	
3	
4	
5	+12V
6	
7	RTN
8	RTN
9	

Table 5-3 Pin Out Connector CN3-1,

Figure 5-4 Power Cable to eInstrument PC

Pin	Signal	Note
1	+12V	Inner Pin CN2-2
2		
3		
4		
5		
6		
7	RTN	Outer Pin CN2-2
8		
9		

Table 5-4 Pin Out Connector CN3-2

5.2 AIS RECEIVER

5.2.1 POWER

HW-REQ-5.2.1.1 The Radio Interface Board shall accept DC power 12V from Battery.

HW-REQ-5.2.1.2 The AIS Receiver shall be responsible for filtering the power supply noise generated by other devices to meet its internal noise requirements.

HW-REQ-5.2.1.3 The AIS Receiver shall consume no more than 6 Watts

HW-REQ-5.2.1.4 The AIS Receiver shall use one connector (9 pin Sub-miniature D plug) for its base electrical interface with pin outs as defined in Table 5-5. This connector is designated CN1-6.

Pin	Signal
1	+12V
2	
3	
4	
5	+12V
6	
7	RTN
8	RTN
9	

Table 5-5: Power Interface Connector CN1-6 Pin Designation

5.2.2 COMMAND INTERFACE

HW-REQ-5.2.2.1 The AIS Receiver shall incorporate one Parallel Interface Bus as its command and telemetry interface.

HW-REQ-5.2.2.2 The interface bus shall be composed of twelve lines: Serial Clocks, Serial Data, Alarm Status and Chip Select Signals as shown in Table 5-6

HW-REQ-5.2.2.3 All signal lines shall be high impedance when the AIS Receiver is not powered.

HW-REQ-5.2.2.4 The AIS Receiver shall use one 26-pin High Density Sub-miniature D plug for its Interface bus with Pin Outs as defined in Table 5-6. This connector is designated CN1-5.

Pin	Signal	Notes
1	FDIO0	SPI-PLL-DATA
2	FDIO1	SPI-ATTN-DATA
3	FDIO2	SPI-PLL-CLK
4	FDIO3	SPI-ATTN-CLK
5	FDIO4	SPI-RX1-ATTN-CS
6	FDIO5	SPI-RX2-ATTN-CS
7	FDIO6	SPI-RX1-LO1-CS
8	FDIO7	SPI-RX2-LO1-CS
9	FDIO8	SPI-LO2-CS
10	FDIO9	RX1-LO1-ALM
11	FDIO10	RX2-LO1-ALM
12	FDIO11	LO2-ALM
13-26	GND	DGND

Table 5-6: Command Interface Connector CN1-5 Pin Designation

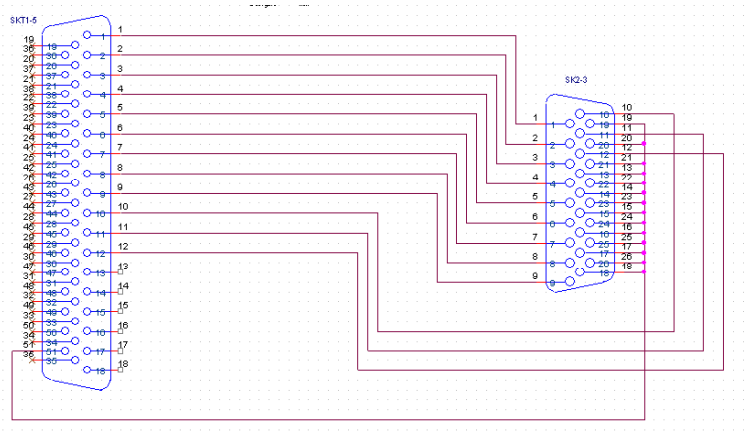

Figure 5-5 Interface Cable

5.2.3 RF INTERFACE

HW-REQ-5.2.3.1 The AIS Receiver shall use one SMA connector. This is designated connector CN1-1.

HW-REQ-5.2.3.2 The AIS Receiver shall maintain emissions at its RF interface in the bands defined in Table 5-7below the levels indicated, referred to its interface connector

Frequency	Emission limit	Description
118.000 MHz – 136.975 MHz	TBD dBm/Hz	TBD
108.000 MHz – 117.975 MHz	TBD dBm/Hz	TBD
225.000 MHz – 319.800 MHz	TBD dBm/Hz	TBD
335.400 MHz – 399.900 MHz	TBD dBm/Hz	TBD
406,375 MHz – 425.000 MHz	TBD dBm/Hz	TBD

Table 5-7: AIS Receiver RF Emission Characteristics

HW-REQ-5.2.3.3 The AIS Receiver shall accommodate RF interference present at it's RF interfaces in the bands defined in Table 5-8 below at the levels indicated

Frequency	Input Power @CN1-1	Description
TBD +/- TBD MHz	TBD dBm	TBD

Table 5-8: Aircraft RF Emission Characteristics

5.2.4 IF INTERFACE

HW-REQ-5.2.4.1 The AIS Receiver shall use two SMA connectors. These are designated SMA connectors CN1-3 and CN1-4.

Pin	Signal
1	Inner Pin Signal
2	Outer Pin Ground

Table 5-9 RF Interface Pin Designations

HW-REQ-5.2.4.2 The two AIS Receiver IF single ended outputs shall be designed for output impedance for 50 Ohms. Table 5-10

Frequency	Level	Description
450 ±25 kHz	± 1Vp-p	@ Maximum input signal

Table 5-10: AIS Receiver IF Output Signals

5.2.5 CLOCK INTERFACE

HW-REQ-5.2.5.1 The AIS Receiver shall use one SMA connector. These are designated connectors CN1-2.

Pin	Signal
1	Inner Pin Signal
2	Outer Pin Ground

Table 5-11 Clock Interface Pin Designations

HW-REQ-5.2.5.2 The AIS Receiver shall be accept Clock Input Level Table 5-12

Frequency	Level	Description
20 MHz	L <= 0.9 V; H <=2.3V	Input Clock

Table 5-12: AIS Receiver Clock Input ModeDigital Unit (eInstrument PC)

5.3 EINSTRUMENT PC

5.3.1 POWER

HW-REQ-5.3.1.1 The Digital Unit shall accept DC power 12 V from Battery.

HW-REQ-5.3.1.2 The Digital Unit shall be consuming no more than 110W under all condition.

HW-REQ-5.3.1.3 The Digital Unit shall use one connector (2 pin socket) for its base electrical interface with pin outs as defined in Table 5-13. This connector is designated CN2-2.

Pin	Signal
1	Inner Pin Signal
2	Outer Pin Ground

Table 5-13: Power Interface Connector CN2-2 Pin Designation

5.3.2 CLOCK INTERFACE X3-TIMING MODULE

HW-REQ-5.3.2.1 The Clock interface shall use one SMA connector with pin outs as defined in Table 5-14. This connector is designated CN2-1.

Pin	Signal
1	Inner Pin Signal
2	Outer Pin Ground

Table 5-14: Clock Interface Connector CN2-1Pin Designation

HW-REQ-5.3.2.2 Output Clock Interface shall be accept 0.85V p-p @50Ω

HW-REQ-5.3.2.3 The Output clock shall be designed for 20 MHz

5.3.3 IF INTERFACE

HW-REQ-5.3.3.1 The eInstrument PC shall use two Analogs to Digital Converters. One Converter for AIS Channel 1 and the other for the AIS Channel 2

HW-REQ-5.3.3.2 The sampling rate should be at 1.800 MHz Samples per second

HW-REQ-5.3.3.3 The minimum precision should be 14 bit.

HW-REQ-5.3.3.4 The IF Inputs (A/D Converter inputs) shall be accept a maximum Input level +/-1Vp-p, and have an impedance of 50Ω.

HW-REQ-5.3.3.5 The IF Inputs shall be connected to SMA connectors (CN2-4, CN2-5).

Pin	Signal
1	Inner Pin Signal
2	Outer Pin Ground

Table 5-15: IF Interface Connectors CN2-4, CN2-5 Pin Designation

5.3.4 GPS INTERFACE

HW-REQ-5.3.4.1 The GPS Module shall be compatible and operate with a standard GPS active antenna.

HW-REQ-5.3.4.2 The GPS Receiver shall be designed for Clock instability < ± 1ppm

HW-REQ-5.3.4.3 The GPS Antenna shall use SMA connector (CN2-6).

Pin	Signal
1	Inner Pin Signal
2	Outer Pin Ground

Table 5-16: GPS Antenna CN2-6 Pin Designation

5.3.5 COMMAND INTERFACE

HW-REQ-5.3.5.1 The Digital Unit shall incorporate one Parallel Interface Bus as its command and telemetry interface.

HW-REQ-5.3.5.2 The interface bus shall be composed of twelve lines: Serial Clocks, Serial Data, Alarm Status, and Chip Select Signals as shown in Table 5-17.

HW-REQ-5.3.5.3 All signal lines shall be high impedance when the Unit is not powered.

HW-REQ-5.3.5.4 The data interface is an unprotected I/O interface. Input voltage must not exceed 4.0 V.

HW-REQ-5.3.5.5 The Digital unit shall use one connector 51-pin Micro D Plug for its Interface bus with Pin Outs as defined in Table 5-17. This connector is designated CN2-3.

Pin	Signal	Notes
1	FDIO0	SPI-PLL-DATA
2	FDIO1	SPI-ATTN-DATA
3	FDIO2	SPI-PLL-CLK
4	FDIO3	SPI-ATTN-CLK
5	FDIO4	SPI-RX1-ATTN-CS
6	FDIO5	SPI-RX2-ATTN-CS
7	FDIO6	SPI-RX1-LO1-CS
8	FDIO7	SPI-RX2-LO1-CS
9	FDIO8	SPI-LO2-CS
10	FDIO9	RX1-LO1-ALM
11	FDIO10	RX2-LO1-ALM
12	FDIO11	LO2-ALM
13	FDIO12	Not in use
14	FDIO13	Not in use
15	FDIO14	Not in use
16	FDIO15	Not in use
17	FDIO16	Not in use
18	FDIO17	Not in use
19	FDIO18	Not in use
20	FDIO19	Not in use
21	FDIO20	Not in use
22	FDIO21	Not in use
23	FDIO22	Not in use
24	FDIO23	Not in use
25	FDIO24	Not in use
26	FDIO25	Not in use
27	FDIO26	Not in use
28	FDIO27	Not in use
29	FDIO28	Not in use
30	FDIO29	Not in use
31	FDIO30	Not in use
32	FDIO31	Not in use
33	FDIO32	Not in use
34	FDIO33	Not in use
35	FDIO34	Not in use

36	FDIO35	Not in use
37	FDIO36	Not in use
38	FDIO37	Not in use
39	FDIO38	Not in use
40	FDIO39	Not in use
41	FDIO40	Not in use
42	FDIO41	Not in use
43	FDIO42	Not in use
44	FDIO43	Not in use
45	FDIO44	Not in use
46	FDIO45	Not in use
47	FDIO46	Not in use
48	TRIG5	Not in use
49	DIO38	Not in use
50	TRIG$	Not in use
51	GND	DGND

Table 5-17: Command Interface Connector CN2-3 Pin Designation

5.4 MOUNTING RACK

HW-REQ-5.4.1.1 The AIS Mounting Rack shall be no lager than 485 mm by 550mm by 600mm including all connectors and fixings.

HW-REQ-5.4.1.2 The AIS Mounting Rack, including all connectors, shall have a mass of less than 60kg. The location of the centre of mass shall be within of the geometric centre.

HW-REQ-5.4.1.3 The AIS Receiver is screwed down to the Mounting Rack

HW-REQ-5.4.1.4 The Digital Unit is screwed down to the Mounting Rack.

6. ACCOMMODATION

HW-REQ-6.1.1.1 The AIS Mounting Rack is strapped down onto the pairs of aircraft rails (TBD).

HW-REQ-6.1.1.2 The Battery Pack shall be mounted horizontally in the Mounting Rack. See Figure 6-1.

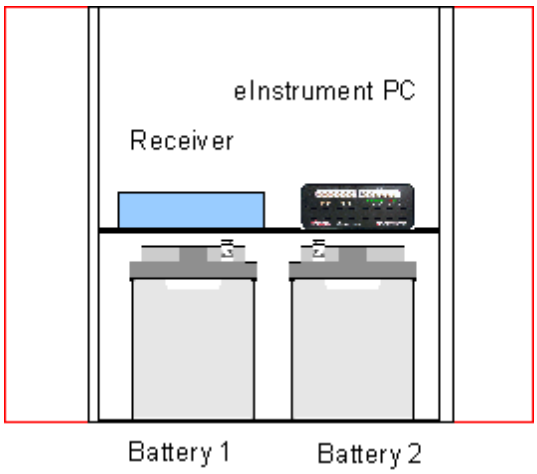

Figure 6-1 Mounting Rack

6.1.2 GROUNDING

HW-REQ-6.1.2.1 The AIS receiver design shall not rely on the aircraft structure for power, signal or returns.

HW-REQ-6.1.2.2 An M4 bonding/grounding stud shall be provided.

HW-REQ-6.1.2.3 The AIS Receiver shall be connected to the second Aircraft VHF- Antenna with a Adaptor cable from SMA to **TBD** (CN1-1, CN0-1)

7. ENVIRONMENTAL REQUIREMENTS

7.1.1 TEMPERATURE RANGE

HW-REQ-7.1.1.1 The AIS Receiver shall meet all performance requirements provided that it is maintained within a range of –0 °C and +50°C during operations and in standby.

HW-REQ-7.1.1.2 The AIS receiver shall generate no more than 6 Watts of heat internally in any operating mode.

HW-REQ-7.1.1.3 The eInstrument PC shall generate no more than 110W of heat internally in any operating mode.

7.1.2 SHOCK AND VIBRATION

HW-REQ-7.1.2.1 Receiver should be sustaining the various vibration and shock levels during flight campaign.

HW-REQ-7.1.2.2 The Data storage (Hard drive) should be sustain the various vibration and shock levels during flight campaign.

ANNEX 1

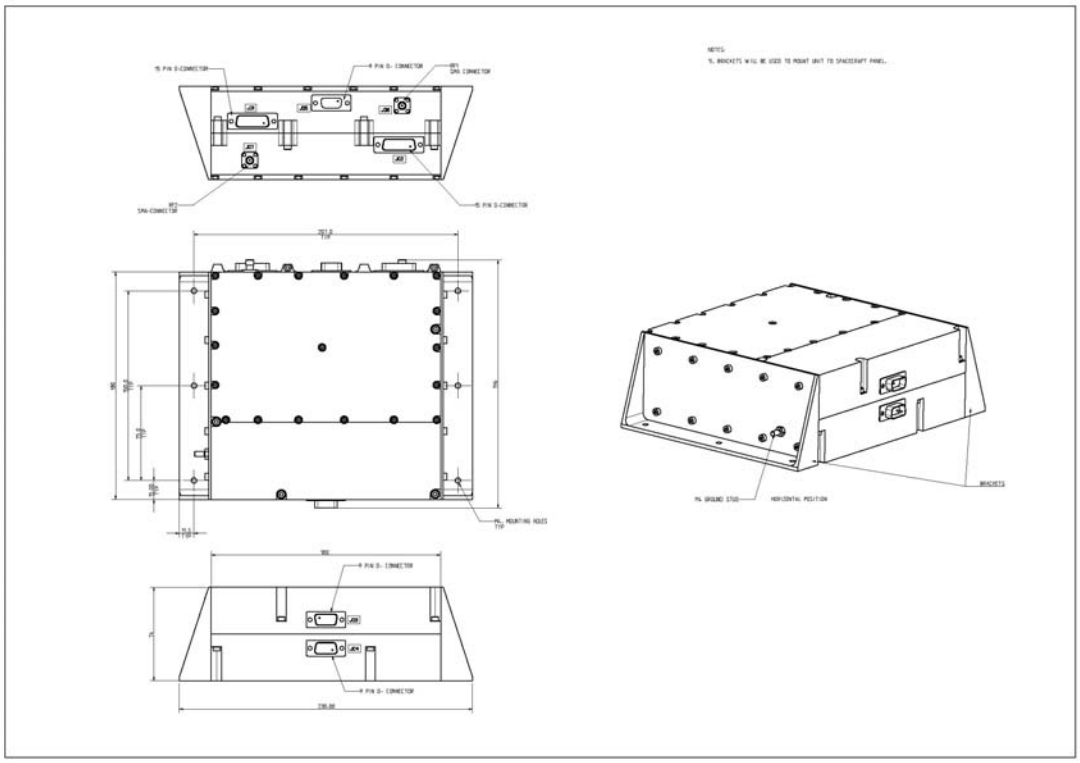

Figure 7-1 Provisional Mechanical Outlines (Place Holder)